19. (New) The leadframe of Claim 17 wherein:

the ring structure includes a ring top surface;

the inner end of each of the leads includes an inner end top surface; and

the inner end top surface of each of the leads is aligned with the ring top surface.

20. (New) The semiconductor package of Claim 17 wherein each of the leads includes a lead transition section extending angularly between the inner end and the frame.

21. (New) The leadframe of Claim 17 further comprising at least one temporary connecting bar connecting the ring structure to the chip mounting pad.

22. (New) The leadframe of Claim 17 further in combination with a non-conductive connector attached to the ring structure and at least one of the leads for maintaining the ring structure in fixed relation to the chip mounting pad and the leads.

Cont'd A1

23. (New) A semiconductor package comprising:

a chip mounting pad defining a peripheral edge;

a semiconductor chip attached to the chip mounting pad and having a plurality of input/output pads;

a plurality of leads, each of the leads including an inner end and an opposed distal end, the inner end of each of the leads being disposed adjacent the peripheral edge in spaced relation thereto and vertically downset relative to the distal end; and

a means disposed along the peripheral edge between the peripheral edge and the inner end of each of the leads for allowing at least two of the input/output pads of the semiconductor chip to be electrically connected to a common one of the leads.

24. (New) The semiconductor package of Claim 23 wherein the means comprises at least

one isolated ring structure which is electrically connected to at least two of the input/output pads of the semiconductor chip and to one of the leads.

25. (New) The semiconductor package of Claim 24 wherein:

the ring structure includes a top ring surface;

the inner end of each of the leads includes an inner end top surface; and

the inner end top surface of each of the leads is aligned with the ring top surface.

Cont'd A1

26. (New) The semiconductor package of Claim 24 wherein:

the semiconductor chip includes a chip top surface;

the inner end of each of the leads includes an inner end top surface; and

the inner end top surface of each of the leads is aligned with the chip top surface.